ABSTRACT

A digital circuit according to the present invention includes a pulse delay circuit where a driving current of an inverter is variable, for causing timing of a clock signal to be variable; and the pulse delay circuit has a stabilizing circuit for an amount of a pulse delay by a delay synchronizing loop, and a generating circuit for a pulse delay amount setting voltage with nonlinear characteristics. The present invention makes it possible to realize a timing delay circuit with high resolution, which is not influenced by an operating environment and requires only a small area for the circuit.